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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,773	01/22/2004	Erik S. Jeng	386998017US1	7535

25096 7590 09/09/2004

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EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,773	JENG, ERIK S.	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05-06-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on May 6, 2004 is being considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 12-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (U.S. Pat. No. 6,734,055).

Regarding claim 12, Lin et al. disclose a method of programming a nonvolatile memory capable of storing multi-bits binary information bits, the memory cell having a plurality of doped regions with a channel and having a gate above the channel, a L-shape dielectric layer formed on side wall of the gate, spacers attached on the L-shape dielectric layer (figure 3), the method comprising: programming a first bit by applying programming voltages to a first doped region of the plurality of doped regions and to the gate while applying programming current or ground potential on a second doped region of plurality of doped regions, thereby injecting and storing electrical charge in a first spacer of the spacers adjacent to the first doped region to represent a first binary status, or to represent a second binary status by not injecting electrical charge into the first spacer (see table of Program, Erase and Read operation, column 5).

Regarding claim 13, Lin et al. disclose the method of claim 12, further comprising: programming a second bit by applying programming voltages to a second doped region of a plurality of doped regions and to the gate, applying the first doped region with programming current or ground potential, thereby injecting and storing electrical charge in a second spacer of the spacers close to the second doped region to represent the first binary status, or to represent the second binary status by not injecting electrical charge into the second spacer (see table).

Regarding claim 14, Lin et al. disclose the method of claim 13, further comprising: programming a third bit by applying programming voltages to a third doped region of the plurality of doped regions and to the gate, applying a fourth doped region of the plurality of doped regions with programming current or ground potential, thereby injecting and storing electrical charge in a third spacer of the spacers close to the third doped region, or to represent the second binary status by not injecting electrical charge into the third spacer (see table).

Regarding claim 15, Lin et al. disclose the method of claim 14, further comprising: programming a fourth bit by applying programming voltages to the forth doped region of the plurality of doped regions and to the gate, applying the third doped region with programming current or ground potential, thereby injecting and storing electrical charge in a fourth spacer of the spacers close to the fourth doped region to present the first binary status, or to represent the second binary status by not injecting electrical charge into the fourth spacer (see table).

Regarding claims 16 and 20, Lin et al. disclose a method of erasing a nonvolatile memory capable of storing multi-bits binary information bits, the memory cell having a first doped region and a second doped region with a channel and having a gate above the channel, a L-shape dielectric layer formed on side wall of the gate, spacers attached on the L-shape dielectric layer

(see figure 3), the method comprising: erasing a first bit of the multi-bits binary information bits by applying erasing voltages to the gate and a first doped region such that to cause charge representing a first binary status to be removed from a first spacer of the spacers for charge trapping (see table, column 5).

Regarding claim 17, Lin et al. disclose the method of claim 16, further comprising: erasing a second bit of the multi-bits binary information bits by applying erasing voltages to the gate and a second doped region such that to cause charge representing a second binary status to be removed from a second spacer of the spacers for charge trapping (see table).

Regarding claim 18, Lin et al. disclose a method of reading an nonvolatile memory capable of storing multi-bits binary information bits, the memory cell having a first doped region and a second doped region with a channel and having a gate above the channel, an L-shape dielectric layer formed on side wall of the gate, spacers attached on the L-shape dielectric layer (see figure 3), the method comprising: applying a reading bias on the gate and a second doped region, the reading bias having levels lower than the voltages applied during programming for sensing a channel current to determine whether the channel current is significantly representing a first binary status in the spacer adjacent to the first doped region or the channel current is relative low to the significant channel current representing a second binary status in the spacer adjacent to the first doped region (see table, column 5).

Regarding claim 19, Lin et al. disclose the method of claim 18, further comprising: applying the reading bias on the gate and a first doped region, the reading bias having levels lower than the voltages applied during programming for sensing the channel current to determine whether the channel current is significantly representing the first binary status in the spacer

adjacent to the second doped region or the channel current is relative low to the significant channel current repressing the second binary status in the spacer adjacent to the second doped region (see table, column 5).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (571) 272-1773.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
August 31, 2004

Gene N Auduong
Primary Examiner
Art Unit 2818